IN THE CLAIMS

1. (Currently amended) A semiconductor storage device comprising:

an amplifier that is activated corresponding to a control signal and amplifies the potential difference between a first node and a second node;

a first switch circuit that is connected between a first bit line and said first node and is controlled to the OFF state after activation of said amplifier; [[and]]

a second switch circuit that is connected between a second bit line and said second node and is controlled to the OFF state after activation of said amplifier; and

a delay circuit that outputs said control signal with a prescribed delay time and, by means of an output signal of said delay circuit, said first switch circuit and said second switch circuit are controlled to be OFF.

2. (Cancelled)

3. (Original) The semiconductor storage device of Claim 1, wherein said first switch circuit and said second switch circuit have a p-type MOS transistor and an n-type MOS transistor coupled together in parallel, and said p-type MOS transistor and n-type MOS transistor are controlled to be OFF at the same time.

4. (Original) The semiconductor storage device of Claim 1, wherein said amplifier has a first inverter coupled between said second node and said first node, a second inverter coupled between said first node and said second node, and a switching element that responds to said control signal and couples said first inverter and said second inverter to a power source.

5. (Original) The semiconductor storage device of Claim

1, further comprising a first charging circuit which is coupled to said first bit line and said second bit line and which charges said first bit line and said second bit line to a prescribed potential.

6. (Original) The semiconductor storage device of Claim 5, further comprising a second charging circuit which is coupled to said first node and said second node and which charges said first node and said second node to a prescribed potential.

7. (Original) The semiconductor storage device of Claim 6, wherein the charging operation of said first charging circuit and said second charging circuit comes to an end before activation of said amplifier.

8. (Original) The semiconductor storage device of Claim 6, further comprising a first data write circuit coupled to said first bit line and a second data write circuit coupled to said second bit line.